1/5 Inch 2 Mega CMOS Image Sensor
SP2518

Specification

Version Commercial 1.7

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SuperPix Micro Technology Co., Ltd

1/5 Inch 2 Mega CMOS Image Sensor Part Number SP2518

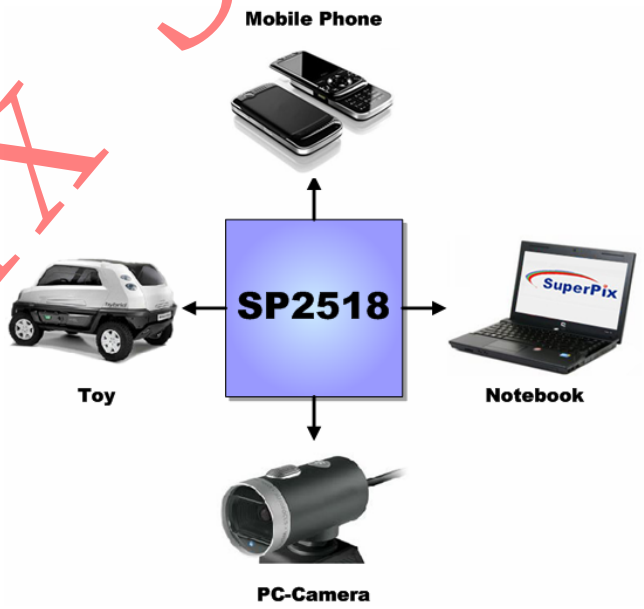
SuperPix™ SP2518 image sensor is one of SuperPix™ 2 Mega Digital image sensor series products. These series sensors have the same maximum image format, UXGA, which means they can be adapted by lots of different kinds of portable equipment, for instance, mobile phones or notebooks. The SP2518 is the newest one of this series, which is based on the 3rd generation 1.75um CMOS image sensor pixel architecture designed by SuperPix™, offering high performance images, making it an ideal choice for mainstream phones. An additional SPI function let SP2518 can access image data from other sensor, which make it can be capable of multi-sensor products.

Functionalities

- CMOS Image Sensor
- Image Signal Processor

Applications

- Mobile Phone
- Notebook
- PC-Cam
- Web-Cam
- Digital Camera
- Toys



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Overview

General Description

SuperPix™ SP2518 image sensor is one of SuperPix™ 2-megapixel Digital image sensor series products. These series sensors have the same maximum image format, UXGA, which means they can be adapted by lots of different kinds of portable equipment, for instance, mobile phones or notebooks. The SP2518 is the newest one of this series, which is based on the 3rd generation 1.75um CMOS image sensor pixel architecture designed by SuperPix™, offering high performance images, making it an ideal choice for mainstream phones. An additional SPI function let SP2518 can access image data from other sensor, which make it can be capable of multi-sensor products. When it works with SuperPix™ SP0827, they can provide high cost performance dual sensor solution.

A high performance system on a chip (SOC) sensor, SP2518 is a chip built on SuperPix™ proprietary pixel and ISP technology for the users who demand high quality sensor for multiple realms. SP2518's image signal processor module includes automatic exposure control, gain control, white balance, black level calibration, lens correction, defect pixel canceling and more. Additionally, it also features all standard image quality controls such as color saturation, hue, gamma, sharpness (edge enhancement) and noise cancellation. Camera controls are accessed over a standard serial camera control bus interface. Other key image processing features include binning functionality that minimizes spatial artifacts and removes image artifacts around edges to deliver clean, crisp images, critical for achieving best-in-class 2-megapixel images. Moreover, SuperPix™'s proprietary sensor technology utilizes advanced algorithms to cancel Vertical Fixed Pattern Noise (VFPN), eliminate smearing, and drastically reduce blooming.

Extending the company's portfolio of 2-megapixel sensor, the 1.75um pixel architecture enables the SP2518 to offer high performance imaging and high definition video in an ultra-compact 1/5 inch optical format, making it an ideal choice for mainstream handset equipments. The advanced pixel architecture

delivers excellent low-light performance for the next generation of high performance mobile phones or PCs.

SP2518 operates at high frame rates, offering SVGA resolution at 30 frames per second (fps), and UXGA resolution at 12 frames per second (fps). SP2518 comes with a standard serial I^2C interface and a high speed parallel output interface delivering RAW or YUV or RGB image data.

An overview of the SP2518 Image Sensor features and functions will be given below.

Function Diagram

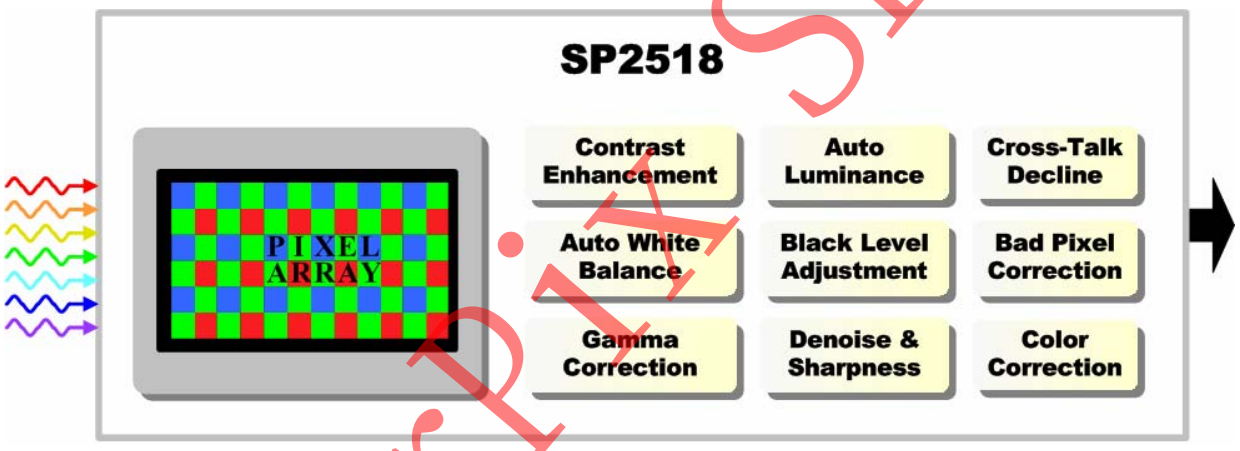


Figure 1 Function Diagram

Typical Application List

- Mobile Phone
- Notebook
- PC-Cam
- Web-Cam
- Digital Camera
- Toys

Typical Application Diagram

Figure 2 Typical Application

Key Performance Parameters

Parameter	Value
Active Pixel Array	1600 x 1200
Pixel Size	1.75um x 1.75um
Active Image Size	2.91 mm x 2.17mm
Lens Size	1/5 inch
Power Supply	I/O 1.8V ~ 3.0V
	Core 1.2 VDC ± 5%
	Analog 2.6V ~ 3.0V
Power consumption	Active 220 mW
	Standby 60 uA
Output Data format	Raw Bayer Format
	YUV422
	RGB565
Max Working Clock	62MHz
Max. Frame Rate	13fps@1600 x 1200 Mode
	30fps@1280 x 720 Mode
	47fps@800 x 600 Mode
	30fps@Binning Mode
Dark Current @ 60°C	40ele/sec
SNR max	38dB
Shutter	Rolling shutter
Operating Temperature	-20°C ~ 70°C
Stable Temperature	0°C ~ 50°C
Package	COB / TSV

Table 1 Key Performance Parameters

Features List

- Active pixel array 1600 x 1200
- Support for UXGA, SVGA
- Analog gain rage is 1.0x – 15.5x
- The image can be zoomed in and zoomed out from 1600 x 1200 to 60 x 60
- Support for video operations
- Support for horizontal and vertical sub-sample
- Embedded black level control
- Support R, Gr, B, Gb 4 transmission channel in analog portion
- Support VFPN reduction circuit
- Embedded image preprocessor functionality
  - Interpolation arithmetic
  - Bad pixel detection and cancellation
  - Auto white balance
  - Auto exposal control
  - Auto black level calibration
  - Image sharpening
  - Smooth inhibiting noise
  - Color space transform
  - Color saturation control
  - Hue control
  - Programmable gamma control
  - Lens correction
  - Defective pixel canceling
  - Noise canceling
- I²C bus controlling registers inside chip
- Support maximum 62MHz working clock
- Support Globe digital gain control
- Pipeline ADC output 10bit image data
- Support strobe signal in order to control flash lamp
- Support SPI interface data access

Function Description

Pixel Array Structure

The SP2518 pixel array is configured as of 1608 columns by 1208 rows, shown below. There are 1600 columns by 1200 rows of optically active pixels.

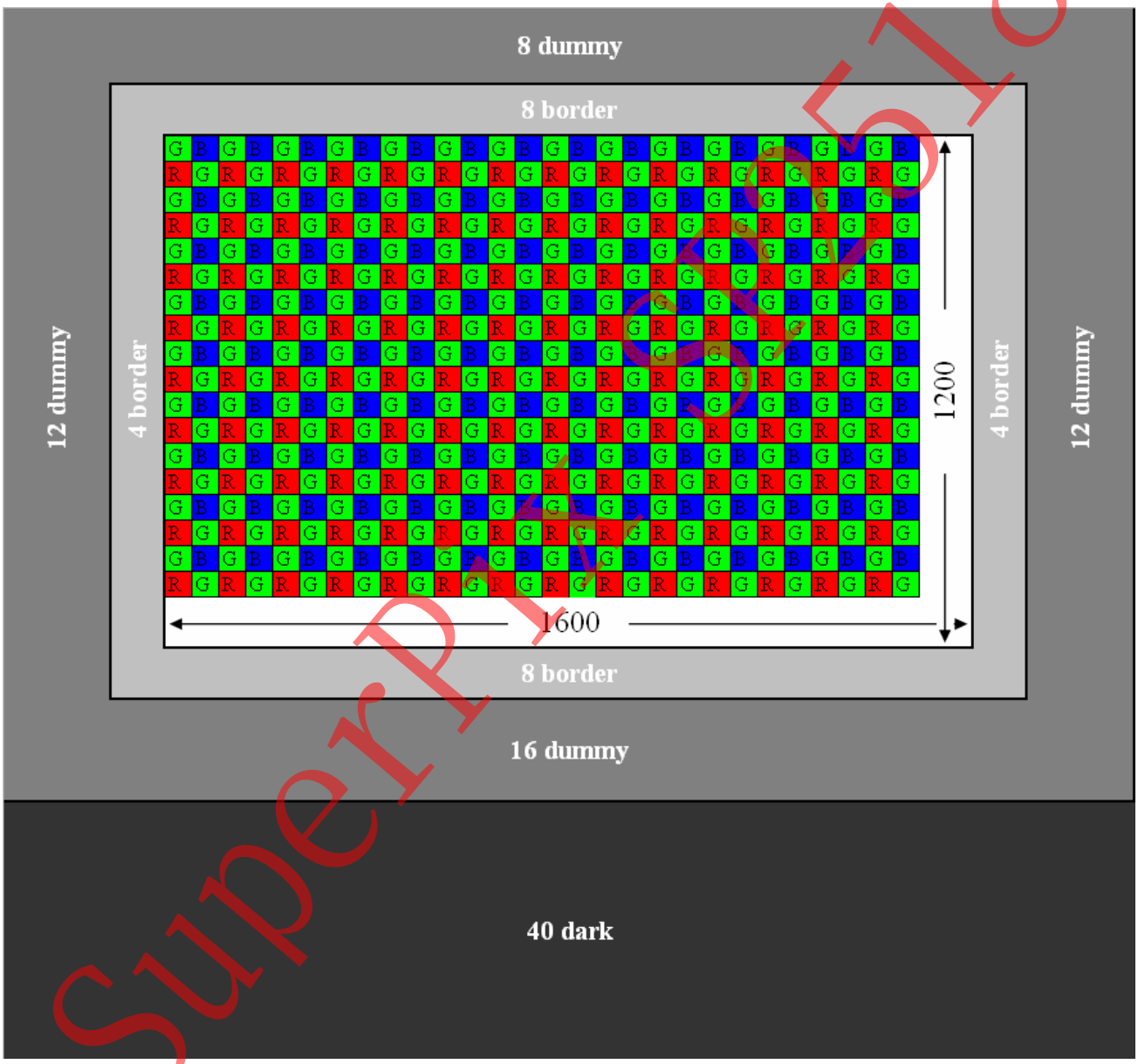


Figure 3 Pixel Array Structure Detail

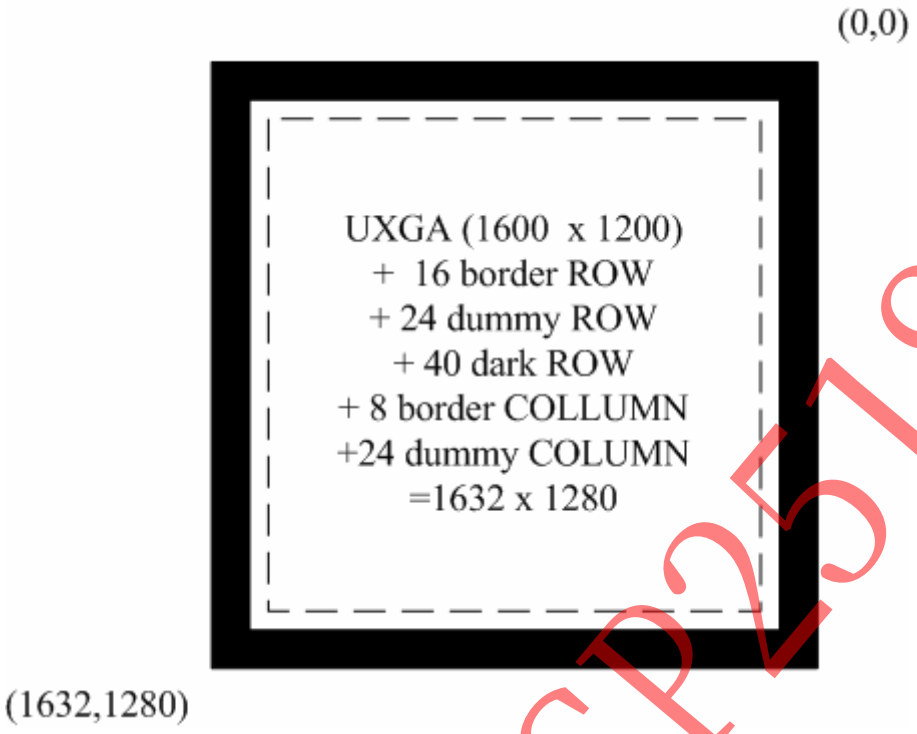


Figure 4 Sensor Pixel Description

Image Signal Process

Black Level Compensation

Image signal processor starts the image processing stream with black level compensation module. The Black level compensation module provides the function which is to adjust the black level of the image from the sensor automatically.

Lens Shading Correction

Lens shading correction unit is used to correct the brightness near the edge of the lens, and make the brightness across the field of view similar. SP2518 has an embedded lens shading correction module that can be programmed to precisely counter the shading effect of a lens on each RGB color signal. The Lens Shading Correction module multiplies RGB signals by a 2-dimensional correction function F(x,y), whose profile in both x and y direction is a piecewise quadratic polynomial with coefficients independently programmable for each direction and color.

Bad Pixel Correction

Bad pixels will be detected and be replaced by a value calculated from the neighbor

pixel during the Bad Pixel module.

Smooth and Sharpness

In this module, smoothing is used to remove the noise in planes and sharpness is used to enhance the edges and detail regions. This block is designed especial for images token out door. The sharpness module of SP2518 is integrated in color interpolation module.

Color Interpolation

Color interpolation module is to convert the raw data to RGB image data. The algorithm is a digital image process used to interpolate a complete image from the partial raw data received form the color filter in form of a matrix of colored pixels. Each 10bit raw pixel data is converted to RGB value using an edge-sensitive color interpolation algorithm.

Auto White Balance

Auto white balance unit is help to remove the unrealistic color from the image automatically by referencing the white balance pre-gain. With auto white balance unit, the still / video camera system can determine the color temperature of the light and automatically adjust for the color temperature.

Color Correction

Color correction unit is design to correct the color with the color correction coefficient. The color correction multiplies the interpolated RGB value by programmable 3x3 matrix to map the color response of the sensor to a desired target. The matrix values are determined based on the spectral response and the cross talk characteristics of the sensor and the values can be programmable. This module can deliver vivid images for users.

Gamma Correction

The SP2518 includes a module for gamma correction that has the capability to adjust its gamma curve, to enhance the performance under certain lighting conditions. As a result, the images turn to more fresh after this module.

RGB to YUV

After the gamma correction, the image data stream undergoes RGB to YUV conversion. The RGB format image data can be turned to YUV422 format.

I²C Bus

Single READ and Single WRITE

The SP2518 I²C write address is 60H and read address is 61H. A typical READ or WRITE sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a WRITE and a 1 indicates a READ. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a WRITE, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

Tow figures that is shown below will illustrate SP2518 single READ sequence and single WRITE sequence.

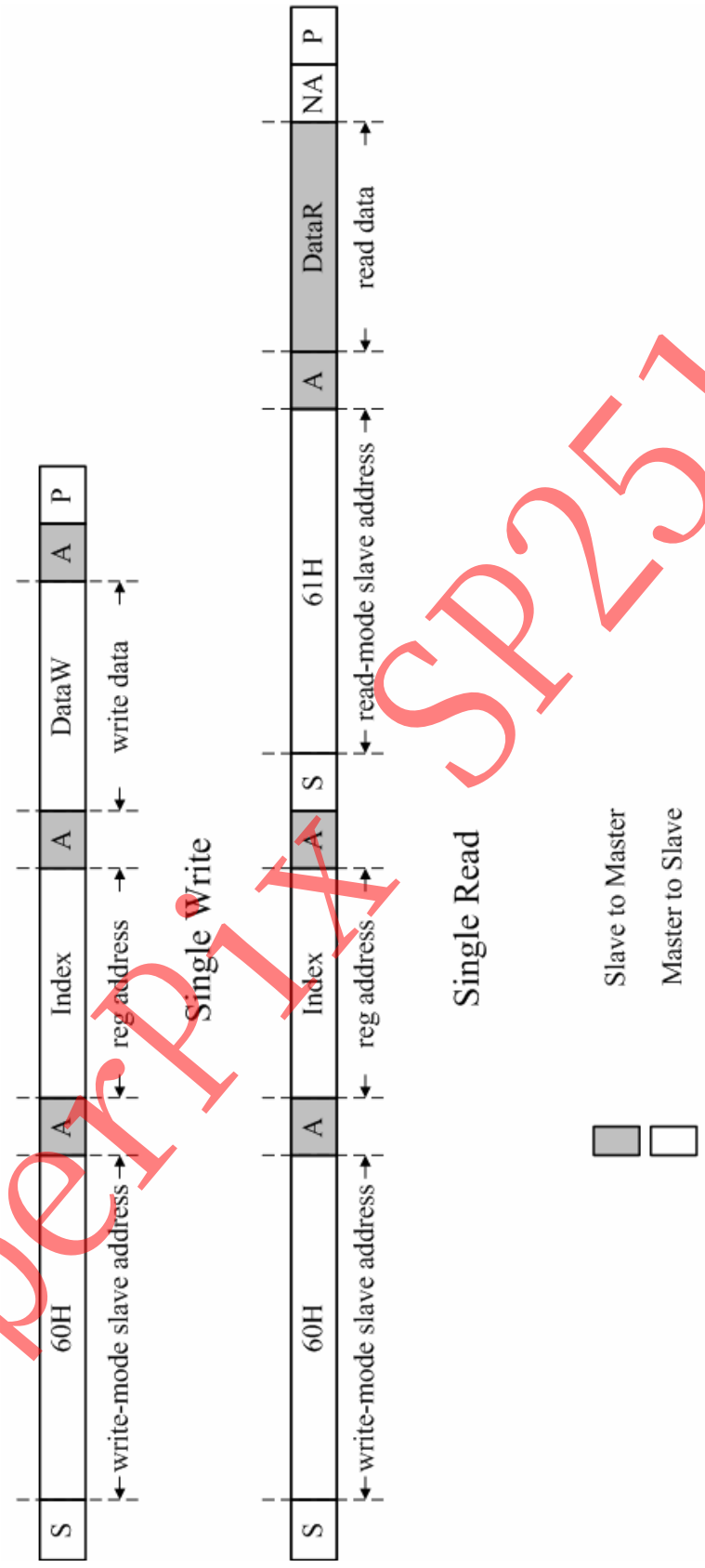


Figure 5 I²C Read & Write Description

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock – it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The SP0838 will hold the value of the SDA pin to logic 0 during the logic 1 state of the Acknowledge clock pulse on SCLK.

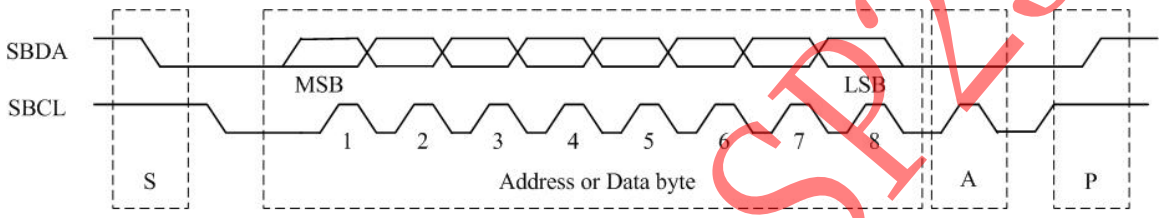


Figure 6 I²C Acknowledge Bit Description

Data Valid

The master must ensure that data is stable during the logic 1 state of the SCLK pin. All transitions on the SDA pin can only occur when the logic level on the SCLK pin is “0”.

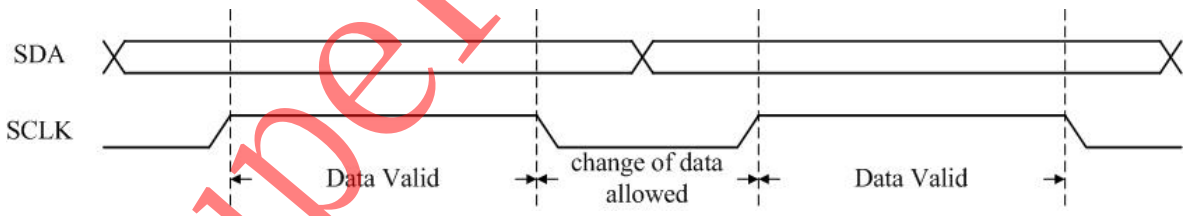


Figure 7 I²C Data Transport Description

Timing Parameter

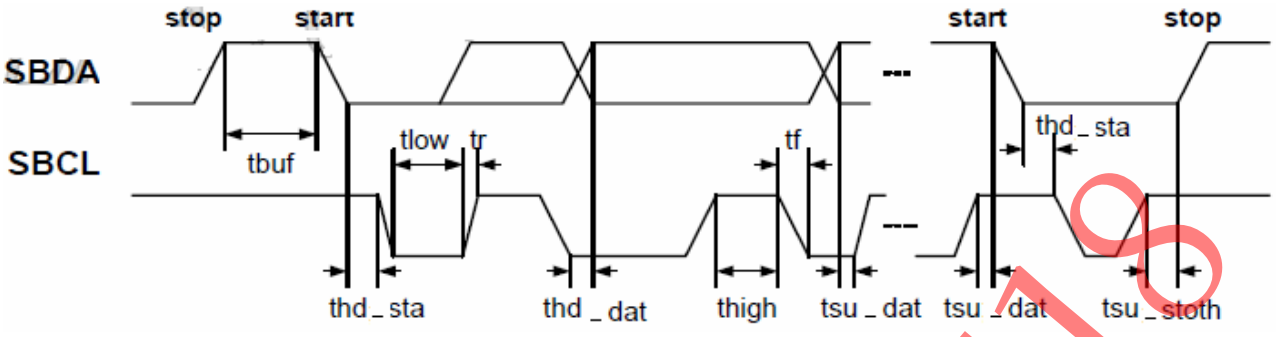


Figure 8 I²C Bus Timing Parameter Illustration

Symbol	Description	Min	Max	Unit
fscl	SBCL clock frequency	0	400	KHz
tbuf	Bus free time between a stop and a start	1.2	-	ns
thd_sta	Hold time for a repeated start	1	-	ns
tlow	LOW period of SBCL	1.2	-	ns
thigh	HIGH period of SBCL	1	-	ns
tsu_sta	Setup time for a repeated start	1.2	-	ns
thd_dat	Data hold time	1.3	-	ns
tsu_dat	Data Setup time	250	-	ns
tr	Rise time of SBCL, SBDA	-	250	ns
tf	Fall time of SBCL, SBDA	-	300	ns
tsu_sto	Setup time for a stop	1.2	-	ns
Cb	Capacitive load of bus line (SBCL, SBDA)	-	-	pf

Electric Characteristics

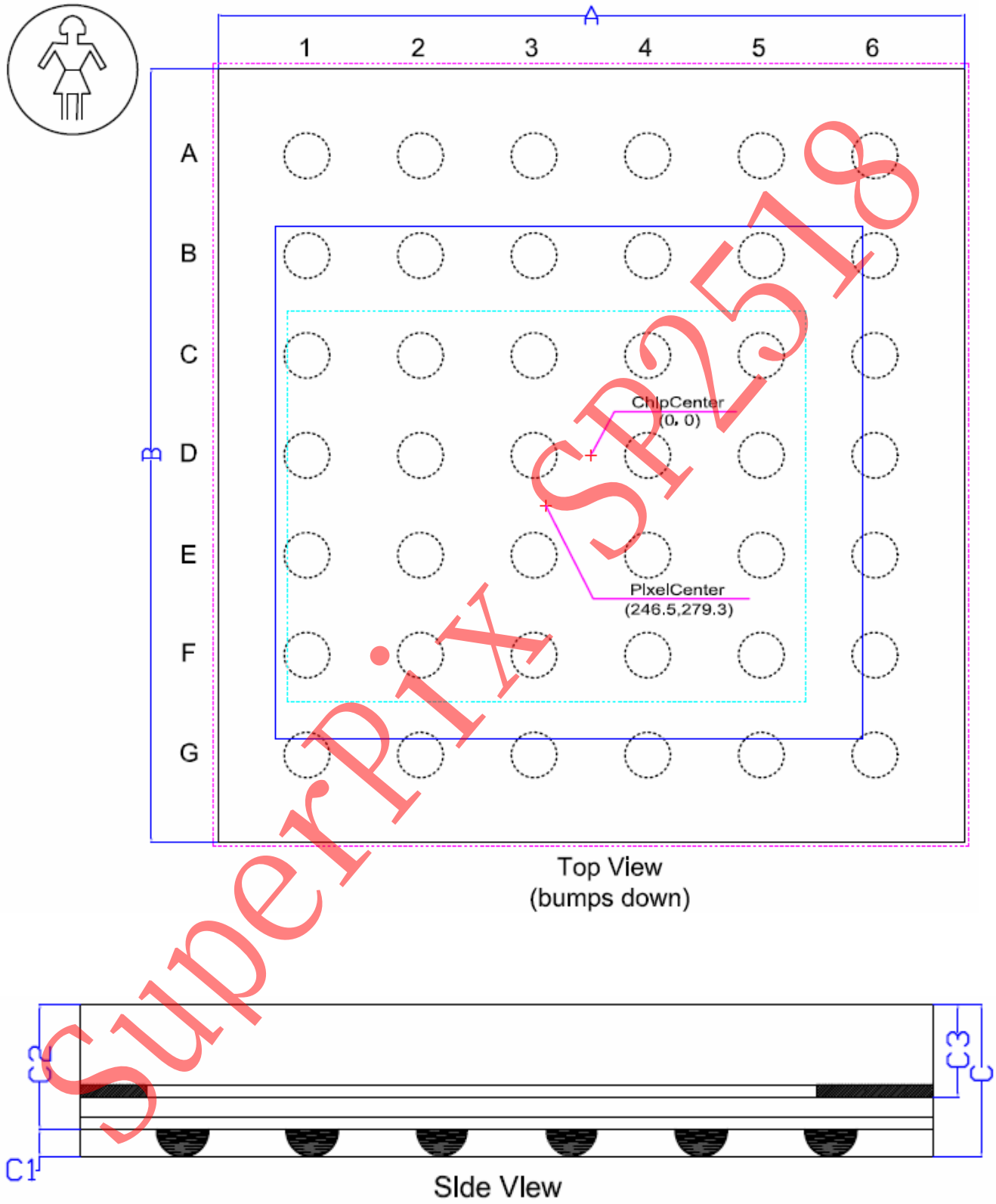
DC Specifications

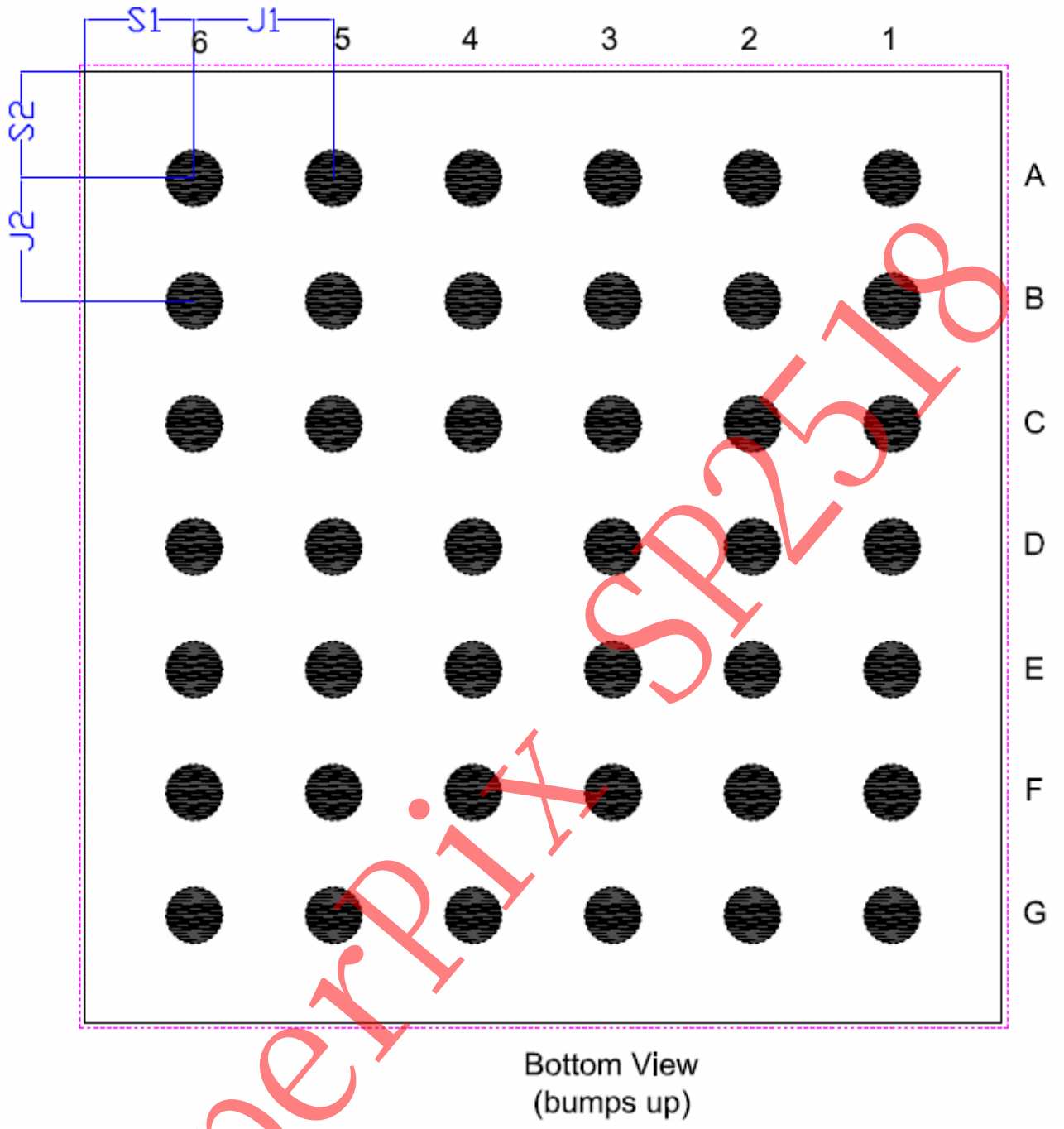
Symbol	Description	Min.	Typ.	Max.	Unit
AVDD	Power supply voltage for IO and analog	2.6	2.8	3.0	V
VDDIO	Power supply voltage for IO and digital	2.6	2.8	3.0	V
		1.6	1.8	2.0	V
VIH	Input high Voltage	0.7xVDDIO		3.0	V
VIL	Input low voltage	0		0.3xVDDIO	V
VOH	Output high voltage@8mA	0.7xVDDIO			V
VOL	Output low voltage@8mA			0.3xVDDIO	V
T	Junction Temperature	-20	25	70	**°C**

Examination Item

No.	Reliability Items	Condition
1	Temp Cycle	-20°C ~ 70°C each 30 min, 24 cycles
2	High Temp. & Humidity storage	70°C / 80% / 72Hr
3	Low Temp. & Humidity storage	-20°C / 96Hr natural dry, for 3 hours
4	High Temp Operating	70°C / 80% / 72Hr / 2.8V other pins are active condition
5	Low Temp Operating	-20°C / 72Hr / 2.8V other pins are active condition
6	Drop Test	1.5m drop, 1 X 6 plane (Camera with 100g cradle)
7	Random Vibration	5~100HZ, 3 axis (X,Y,Z),15min/axis,swing :6mm

Package





	1	2	3	4	5	6
A	D[0]	DVDD28	DGND	PCLK	DGND	DVDD28
B	D[1]	D[2]	D[3]	D[5]	D[7]	D[9]
C	DVDD18	STROBE	D[4]	HSYNC	D[8]	CVDD28
D	DGND	DVDD15	VSYNC	D[6]	DVDD15	AGND28
E	DVDD28	ECLK	BYP_LDO	PD	AGND28	AGND28
F	SDBA	RST	SCLK	\	AGND28	AVDD28
G	AVDD28	AGND28	PVDD28	\	AGND28	AVDD28

Figure 9 Pin Name

Parameter	Symbol	Nominal	Min.	Max.
Package Body Dimension X	A	4105	4080	4130
Package Body Dimension Y	B	4259	4234	4284
Package Height	C	730	670	790
Ball Height	C1	130	100	160
Package Body Thickness	C2	600	565	635
Thickness of glass surface to wafer	C3	445	425	465
Ball Diameter	D	250	220	280
Total Ball count	N	42	–	–
pin pitch X axis	J1	625	–	–
Pin pitch Y axls	J2	550	–	–
Edge to Pin Center Distance along X	S1	490	460	520
Edge to Pin Center Distance along Y	S2	479.5	450	510

Figure 10 Package Dimensions

PIN#	PAD_NAME	I/O	Description	PIN#	PAD_NAME	I/O	Description
A1	D[0]	O	Pixel Array Output Bit 0	D4	D[6]	O	Pixel Array Output Bit 6
A2	DVDD28	DP	Digital I/O Power 2.8V	D5	DVDD15	DP	Digital core power 1.5V, internal only
A3	DGND	DG	Digital Ground				
A4	PCLK	O	Pixel Output Clock	D6	AGND28	AG	Analog Ground
A5	DGND	DG	Digital Ground	E1	DVDD28	DP	Digital I/O Power 2.8V
A6	DVDD28	DP	Digital I/O Power 2.8V	E2	ECLK	I	Input Clock
B1	D[1]	O	Pixel Array Output Bit 1	E3	BYP_LDO	I	"0"Internal Power,"1"External Power
B2	D[2]	O	Pixel Array Output Bit 2	E4	PD	I	Power Down,"0"Normal
B3	D[3]	O	Pixel Array Output Bit 3	E5	AGND28	AG	Analog Ground
B4	D[5]	O	Pixel Array Output Bit 5	E6	AGND28	AG	Analog Ground
B5	D[7]	O	Pixel Array Output Bit 7	F1	SDBA	I/O	Slave Tri-state,I2C Data Bus
B6	D[9]	O	Pixel Array Output Bit 9	F2	RST	I	Rst Signal
C1	DVDD18	DP	Digital Power 1.8V	F3	SCLK	I	Slave I2C Clock Bus
C2	STROBE	O	Strobe Signal	F4	NC		
C3	D[4]	O	Pixel Array Output Bit 4	F5	AGND28	AG	Analog Ground
C4	HSYNC	O	Horizontal Sync Signal	F6	AVDD28	AP	Analog power 2.8V
C5	D[8]	O	Pixel Array Output Bit 8	G1	AVDD28	AP	Analog power 2.8V
C6	CVDD28	CP	Charge-pump power 2.8V	G2	AGND28	AG	Analog Ground
D1	DGND	DG	Digital Ground	G3	PVDD28	PP	Pixel Power 2.8V
D2	DVDD15	DP	Digital core power 1.5V, internal only	G4	NC		
				G5	AGND28	AG	Analog Ground
D3	VSYNC	O	Verticall Sync Signal	G6	AVDD28	AP	Analog power 2.8V

Figure 11 Pin Description

Revision History

Version #	Date	Modification
Commercial 1.0	2011.10.17	1. The first version only for customers.
Commercial 1.1	2011.10.18	1. edit key performance parameters: power consumption, dark current, and SNR.
Commercial 1.2	2011.10.24	1. add package description 2. this version is only for TSV package
Commercial 1.3	2011.11.22	1. edit figure4 2. edit I^2C description
Commercial 1.4	2011.12.08	1. edit application diagram 2. add electric characteristics including DC specifications and examination item 3. edit package and pin description
Commercial 1.5	2011.12.12	1. edit table 2 package dimensions
Commercial 1.6	2012.03.23	1. edit pixel array structure
Commercial 1.7	2012.03.26	1. add Package chapter