



Data Sheet

NT99252

1/5" UXGA CMOS Image Sensor

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1. Features

- Low dark current
- Auto black level calibration
- Two wire serial interface, 16-bit address and 8-bit data
- Support output format: YCbCr (4:2:2) and Raw
- Support image size: UXGA (1600 by 1200) and any size from scaling down
- Lens shading correction
- Automatic control functions: Auto-Exposure control (AE) and Auto-White Balance (AWB)
- Including: Sharpness, noise reduction, defect correction, gamma, color saturation adjustment.
- Special effects included.
- Target module size: 6.5mm x 6.5mm

2. Key Performance

Parameter		Value
Array Size		1604 x 1204
Power Supply	Digital	1.5V ± 5%
	Analog	2.5V ~ 3.1V
	I/O	1.7V ~ 3.1V
Pixel Size		1.75 μm x 1.75 μm
Image Area		2807μm x 2107μm
ADC Resolution		10 bits
Shutter		Electronic Rolling Shutter
Frame rate	SVGA	30 fps
	UXGA	15 fps
Color Filter Arrays		RGB Bayer pattern
Maximum Data Rate		36 Mp/s
Maximum Clock Rate		72 MHz
Power Consumption		TBD mW @15fps, 72MHz, Full Size Standby: < TBDuA

3. General Description

The NT99252 is a high performance image sensor. It incorporates a 1604 (H) x 1204 (V) image array, an on-chip PLL oscillator and an on-chip 10 bits ADC, and embedded image signal processor. All the required image signal processing functions, including sharpness, noise reduction, defect correction, gamma, and color saturation adjust are supported. User can easily control through two-wire serial interface bus.

It is suitable for cellular phones and PC cameras applications.

4. Block Diagram

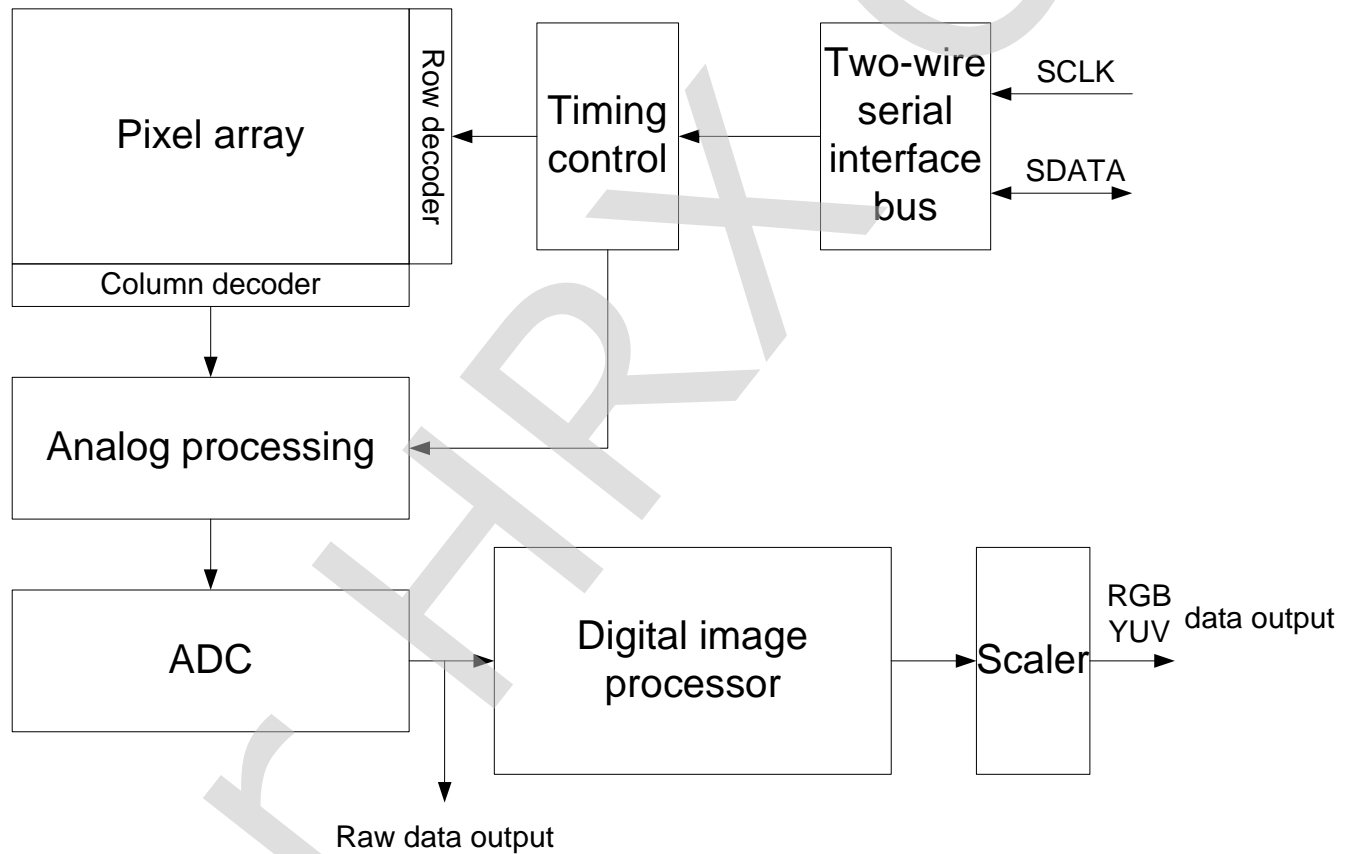


Fig. 1 Block Diagram

5. Pin Configuration

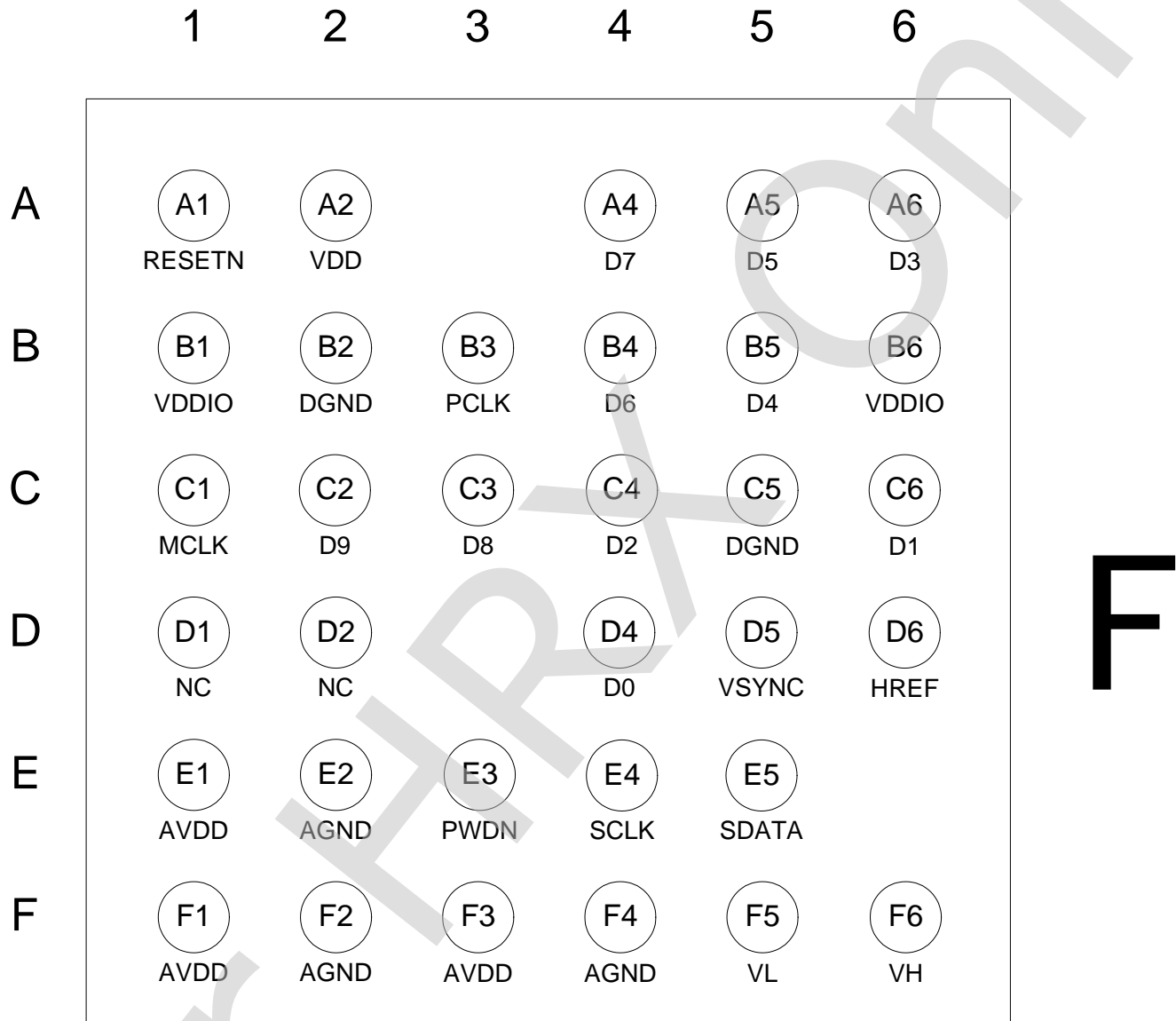


Fig. 2 Pin Configuration (Top View)

6. Pin Descriptions

I = input port

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking

Pin No.	Name	Type	Descriptions
A1	RESETN	I	Power on reset, active low 0: reset 1: normal
A2	VDD	Power	Digital power
A4	D7	O	Data output 7
A5	D5	O	Data output 5
A6	D3	O	Data output 3
B1	VDDIO	Power	Digital power for I/O
B2	DGND	Ground	Digital ground
B3	PCLK	O	Pixel clock output
B4	D6	O	Data output 6
B5	D4	O	Data output 4
B6	VDDIO	Power	Digital power for I/O
C1	MCLK	I	System clock input
C2	D9	O	Data output 9
C3	D8	O	Data output 8
C4	D2	O	Data output 2
C5	DGND	Ground	Digital ground
C6	D1	O	Data output 1
D1	NC	-	NC
D2	NC	-	NC
D4	D0	O	Data output 0
D5	VSYNC	O	Vertical synchronization
D6	HREF	O	Horizontal reference
E1	AVDD	Power	Analog power
E2	AGND	Ground	Analog ground
E3	PWDN	I	Power down mode select, active high 0: normal mode 1: power down mode
E4	SCLK	I	Two-wire serial interface bus clock input
E5	SDATA	I/O	Two-wire serial interface bus data I/O
F1	AVDD	Power	Analog power
F2	AGND	Ground	Analog ground
F3	AVDD	Power	Analog power
F4	AGND	Ground	Analog ground
F5	VL	-	Connect to AGND
F6	VH	-	Connect to AVDD

D[9:0] is 10-bit Raw output(D9: MSB, D0: LSB), D[9:2] is 8-bit YUV output

7. Package Outline

	Symbol	Nominal	Min.	Max.
			μm	
Package Body Dimension X	A	3942	3917	3967
Package Body Dimension Y	B	3992	3967	4017
Package Height	C	790	730	850
Ball Height	C1	160	130	190
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	300	270	330
Total Pin Count	N	33(2NC)		
Pin Count X axis	N1	6		
Pin Count Y axis	N2	6		
Pins Pitch X axis	J1	600		
Pins Pitch Y axis	J2	600		
Edge to Pin Center Distance along X	S1	471	441	501
Edge to Pin Center Distance along Y	S2	496	466	526

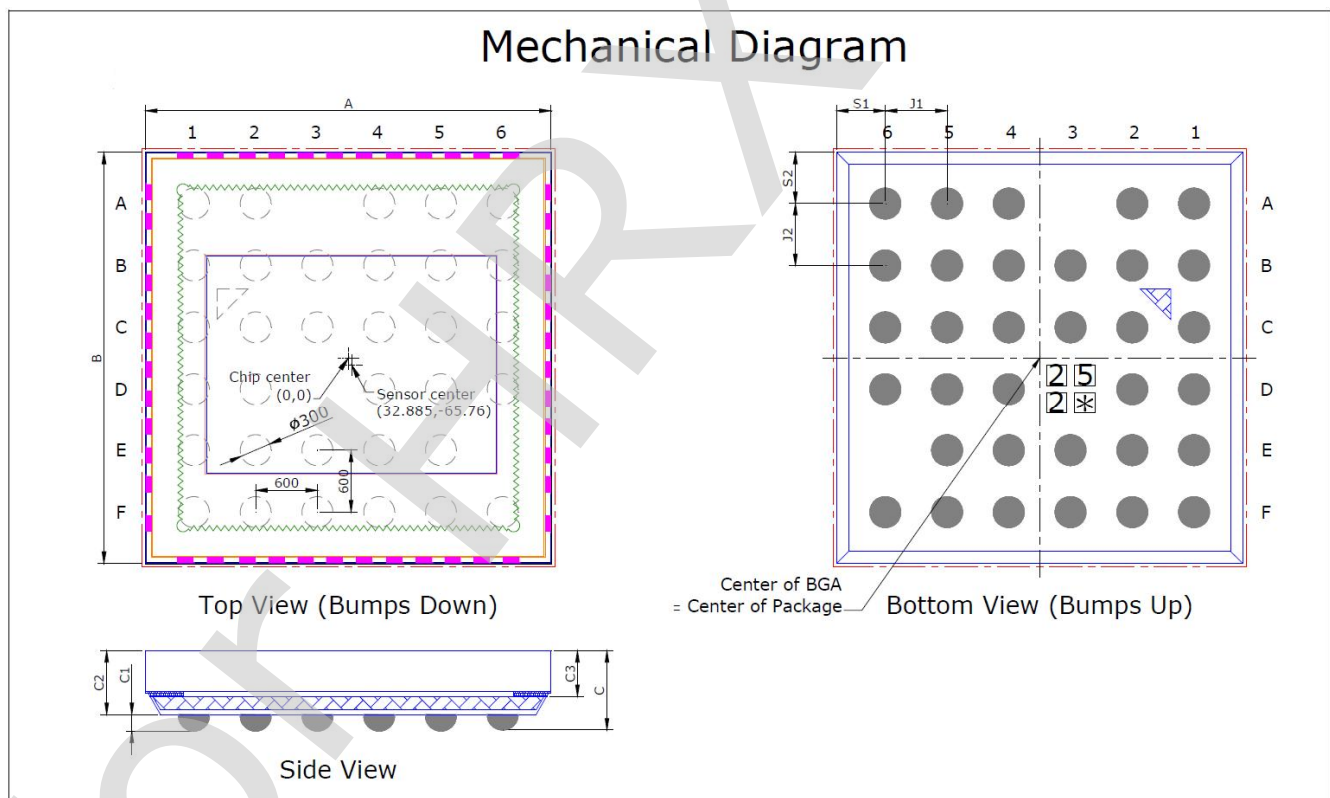


Fig. 3 Package Outline

8. Reference Circuit

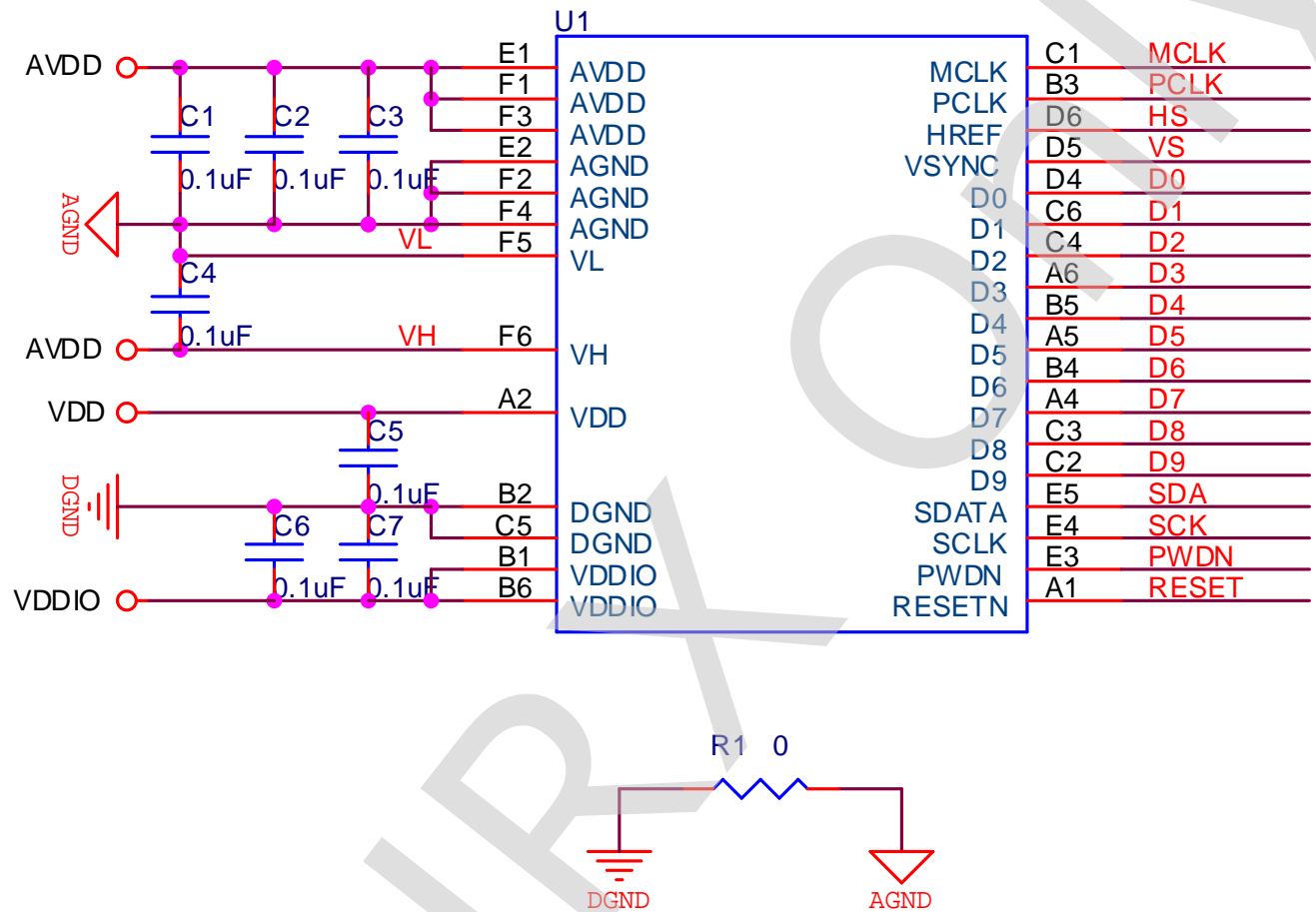


Fig. 4 Reference Circuit

9. Chief Ray Angle

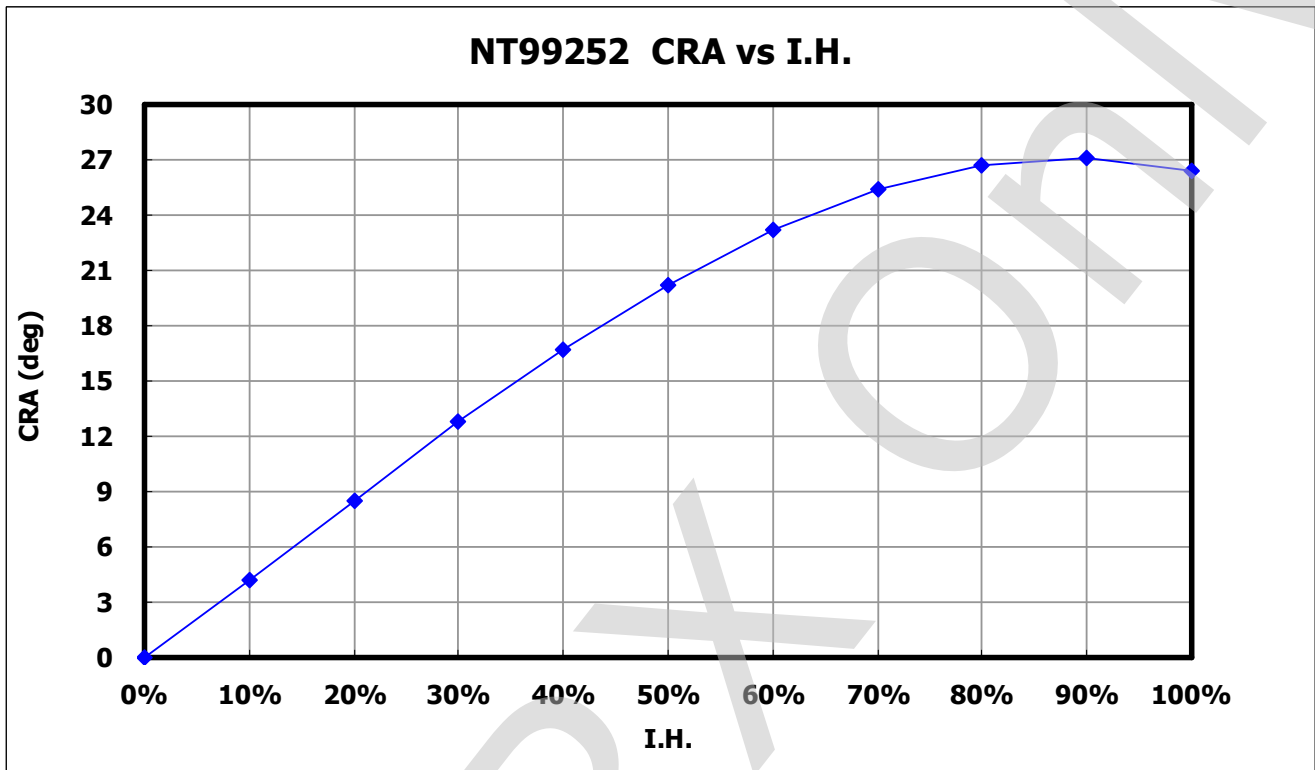


Fig. 5 Chief Ray Angle vs Image Height

10. SMT Reflow Profile

	A	B		C	D		E		F
	Ramp up	Pre-heat		Ramp up	Melt point		Peak point		Ramp down
		Temp.	Time		Temp.	Time	Temp.	Time	
New Reflow Profile	Max 3°C/sec	150 ~ 200°C	60 ~ 70 sec	Max 3°C/sec	217°C	60 ~ 70 sec	235 ~ 240°C	20 ~ 25 sec	Max 6°C/sec

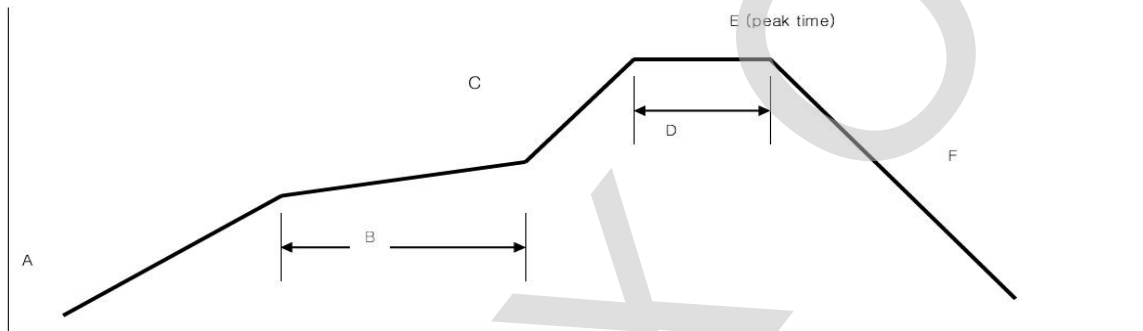


Fig. 6 SMT Reflow Profile